IN THE SPECIFICATION:

Please replace the paragraph on page 1, lines 9-23, with the following amended paragraph:

Increasing demand for portable and other wireless devices has created a greater need for circuits with very low stand-by leakage current. Typically, lower power is achieved through the use of lower ~~supplier~~ supply voltages. Due to this lower supply voltage, power conscious designers have begun to utilize dual threshold voltage (V_t) transistor designs. In a dual V_t circuit, transistors can have either a high or low threshold voltage characteristic. Low V_t devices have approximately twice the switching speed of high V_t devices, but they contribute a leakage power that is several orders of magnitude higher along with a slightly higher capacitance. In order to meet both the leakage and performance requirements of portable devices, a mixture of low and high V_t devices can be used. Unfortunately, conventional design methodologies cannot provide a method for determining which of the transistors in an integrated circuit will be designed as low V_t devices and which will be designed as high V_t devices. It is highly desirable to implement a method for automatically selecting an optimal V_t mixture such that all design constraints are met.

Please replace the paragraph on page 12, lines 3-16, with the following amended paragraph:

Turning now to FIG 4, a flow diagram illustrating a method 306 for determining a DLS of an integrated circuit according to one embodiment of the invention is presented. In the depicted embodiment, a DCC of the circuit is represented in a simplified fashion. Referring also to FIGs 6 and 7A, an exemplary circuit diagram and the corresponding simplified representation suitable for determining DLS's are presented for purposes of illustrating method 306. The circuit representation (FIG 7A) is used to determine a set of partition pairs S_I, T_I for I=0 to N-1 and N represents the number of minimum partitions into which the circuit can be divided. A minimum partition, as used herein, refers to a partition of the circuit in which the circuit includes two connected components, one of which contains a first power supply node and the other of which contains a second power supply node. In one embodiment, the first power supply node may be the Vdd node, while the second power supply node may be the ground node.